OTAs and OPamps

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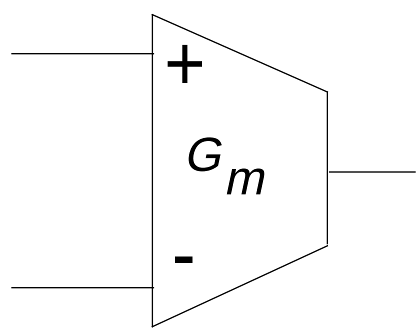
Outline

- *Review - general properties of amplifiers*
- *Simple OTA*
  - *Review*
  - *Design plan*
- *Two-stage amplifier: Miller CMOS OTA*
  - *Characteristics*
  - *Governing equations*
  - *Design plan*
- *One-stage amplifier: Symmetric OTA*
  - *Characteristics*
  - *Design plan*

Definitions

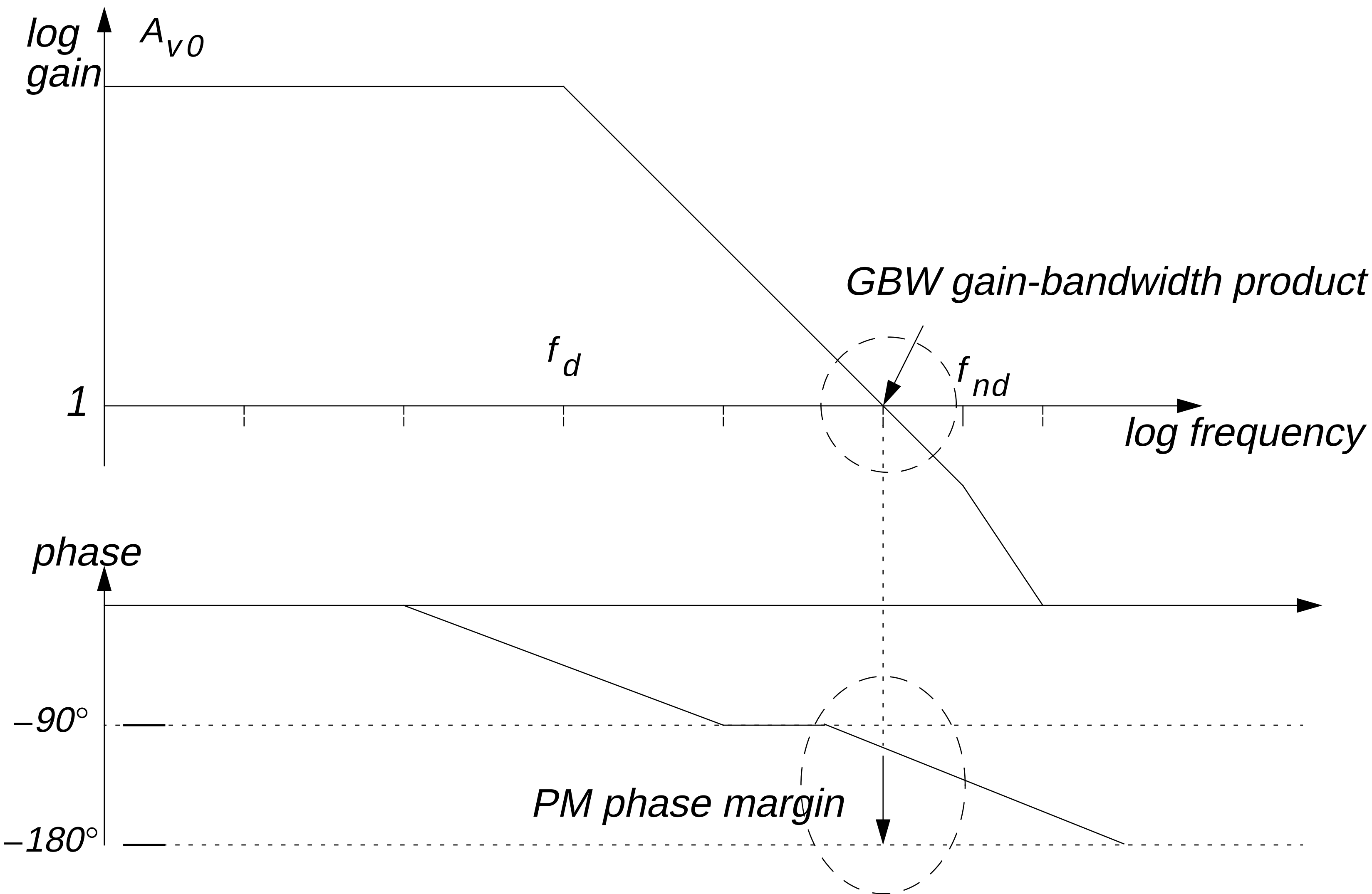
- *OPamp = operational amplifier*
  - *Voltage in-voltage out*
  - *Low output impedance*
- *OTA = operational transconductance amplifier*
  - *Voltage in-current out*
  - *Not so low output impedance*
  - *Still used as voltage amplifier*



Properties of amplifiers

- *gain-bandwidth product*
- *phase margin*
- *open-loop gain*
- *slew rate*
- *input impedance*
- *output impedance*
- *output noise*
- *area*
- *power-supply rejection ratio*
- *common-mode rejection ratio*
- *power consumption*
- *dynamic range*
- *offsets*

Fundamental characteristics



Fundamental design specification

- *GBW gain-bandwidth product*
  - *A_{v0} & GBW specifies location of dominant pole:*

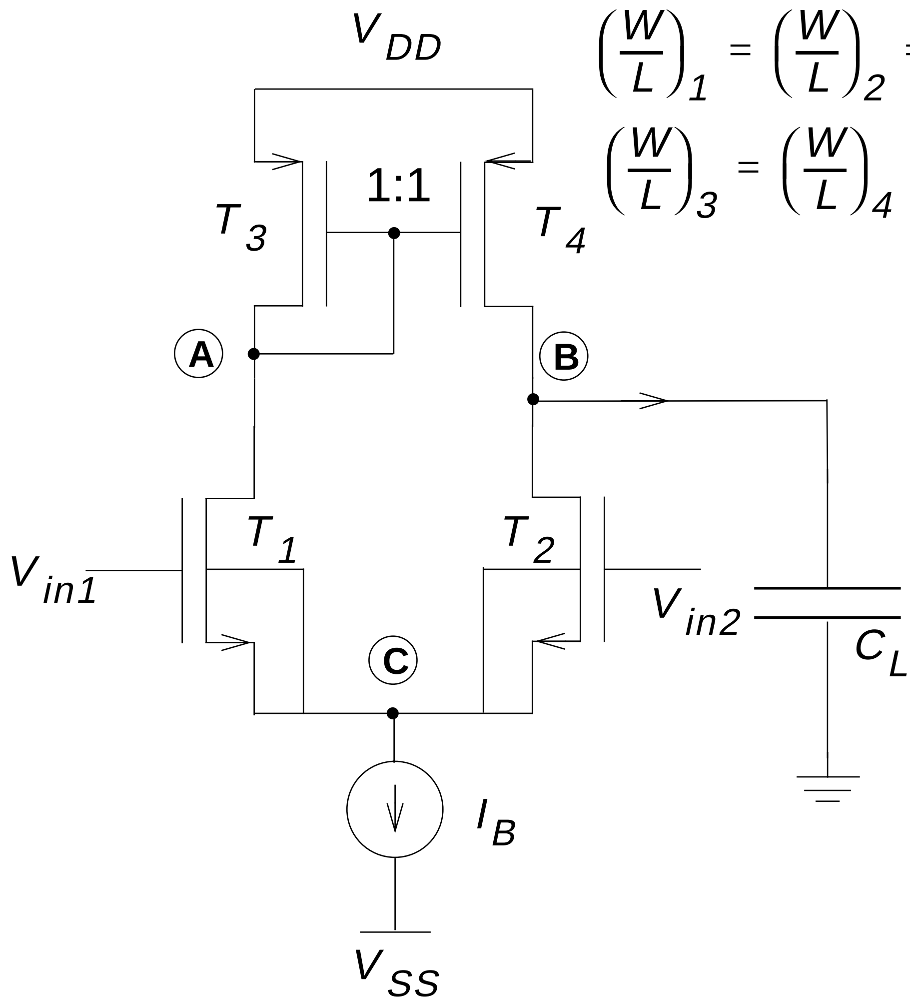
$$f_d = \frac{GBW}{A_{v0}}$$

- *PM phase margin*
  - *specifies location of first non-dominant pole relative to GBW:*

$$f_{nd} = M \cdot GBW \Rightarrow PM = -90° - \operatorname{atan}\frac{1}{M} + 180° = 90° - \operatorname{atan}\frac{1}{M}$$

Useful example: $M = 3 \Rightarrow PM = 90° - 18.4° = 71.6°$

Design of simple OTA



$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_i \qquad g_{m1} = g_{m2} = G_m$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_l \qquad g_{m3} = g_{m4} = g_{ml}$$

$$g_{o1} = g_{o2} = g_{o3} = g_{o4} = g_o$$

$$A_{v0} = \frac{v_{out}}{v_{in}} = \frac{G_m}{g_B}$$

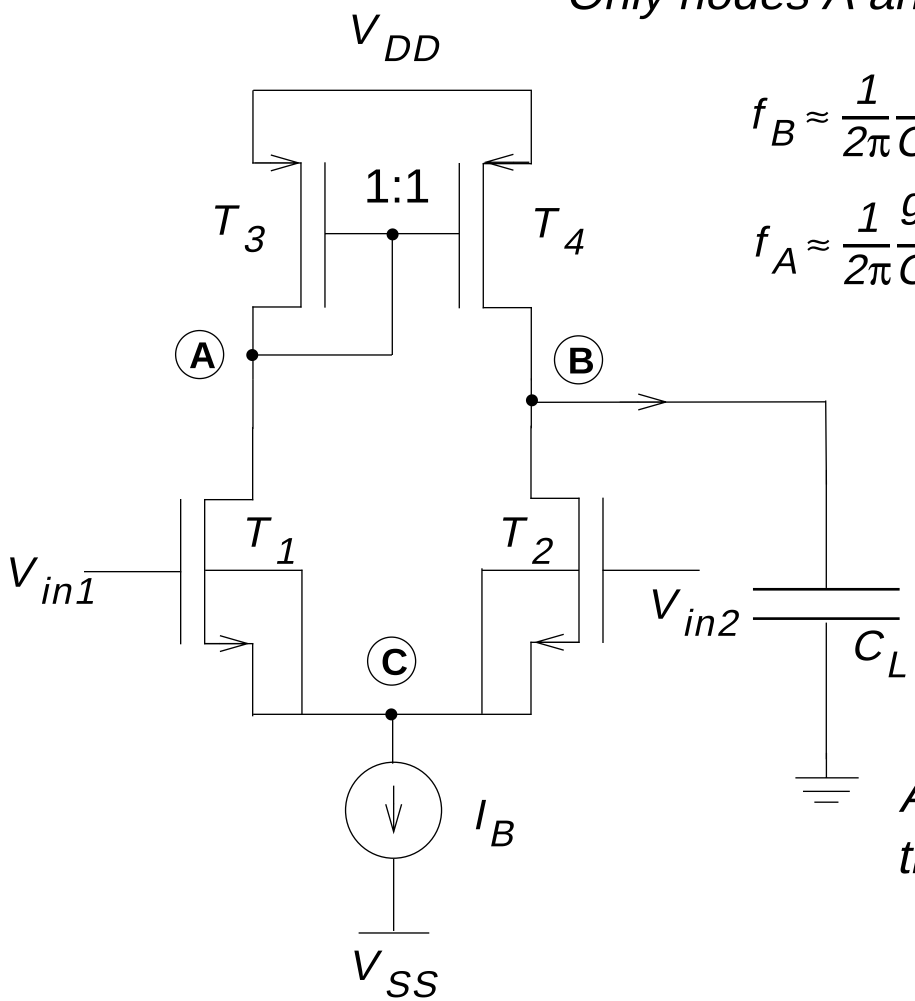
$$G_m = \frac{I_B}{V_{GSi} - V_T}$$

$$g_B = 2g_o = \frac{I_B}{V_{En}L_i}$$

$$A_{v0} = \frac{V_{En}L_i}{V_{GSi} - V_T}$$

Example: $A_{v0} = \frac{4.5 \cdot 10}{0.2} = 225$

GBW of simple OTA



Only nodes A and B influence frequency behavior

$$f_B \approx \frac{1}{2\pi}\frac{g_B}{C_B + C_L} \qquad g_B = 2g_o = \frac{I_B}{V_{En}L_i}$$

$$f_A \approx \frac{1}{2\pi}\frac{g_A}{C_A} \qquad g_A \approx g_{mI}$$

$$C_B \approx C_A$$

Generally $g_m \gg g_o$

so node B dominates

$$GBW = A_{v0}f_d = \frac{G_m}{2\pi(C_L + C_B)}$$

$$f_{nd} \approx \frac{1}{2\pi}\frac{g_{mI}}{C_A}$$

A larger load capacitance increases the distance between the poles!

Design plan for max GBW

Given C_L design a simple OTA with max GBW

Governing equation 1: $$GBW = A_{v0} f_d = \frac{G_m}{2\pi(C_L + C_B)}$$

Set f_{nd} at GBW (that is use PM = 45 ^{o})

Governing equation 2: $$\frac{g_{ml}}{C_A} \approx \frac{G_m}{(C_L + C_B)}$$

Remember from lecture 1:

$$g_m = 2K'\frac{W}{L}(V_{GS} - V_T) = \sqrt{2K'\frac{W}{L}I_D} = \frac{2I_D}{(V_{GS} - V_T)}$$

Three design parameters, for example: $\left(\frac{W}{L}\right)_i, \left(\frac{W}{L}\right)_l, I_B$

But only two equations!

Design plan cont.

Again, remember from lecture 1:

$$g_m = 2K'\frac{W}{L}(V_{GS} - V_T) = \sqrt{2K'\frac{W}{L}I_D} = \frac{2I_D}{(V_{GS} - V_T)}$$

We assume: $K_n' = 2K_p'$

$$f_{nd} \approx GBW \Rightarrow \left(\frac{W}{L}\right)_l \approx 2\left(\frac{W}{L}\right)_i\left(\frac{C_A}{C_L + C_B}\right)^2$$

We have two design parameters left to choose:

$$GBW = \frac{\sqrt{2K_n' I_B}}{2\pi}\frac{\sqrt{(W/L)_i}}{(C_L + C_B)}$$

GBW vs. W/L_i for variable I_B

Modified design equations

Node capacitance is not independent of transistor sizes!

Use: $\frac{W}{L} \equiv r \qquad C_n = C_{n0} + k \cdot r$

$$C_B = C_L + C_{n0B} + k \cdot (r_i + r_l) = C_L' + k \cdot (r_i + r_l)$$

$$C_A = C_{n0A} + k \cdot (r_i + r_l)$$

$$GBW = \frac{\sqrt{2K_n' I_B}}{2\pi} \frac{\sqrt{r_i}}{C_L' + k \cdot (r_i + r_l)}$$

$$\frac{r_l}{2r_i} = \sqrt{\frac{C_{n0A} + k \cdot (r_i + r_l)}{C_L' + k \cdot (r_i + r_l)}}$$

Modified GBW vs. W/L_i for variable I_B

Final design choices

Optimum is obtained at: $\left(\frac{W}{L}\right)_i = 18.3 \Rightarrow \left(\frac{W}{L}\right)_l \approx 5$

$$GBW_{max} = \frac{1}{2}\frac{\sqrt{2K_n'I_B}}{2\pi}\frac{1}{\sqrt{3kC_L'}}$$

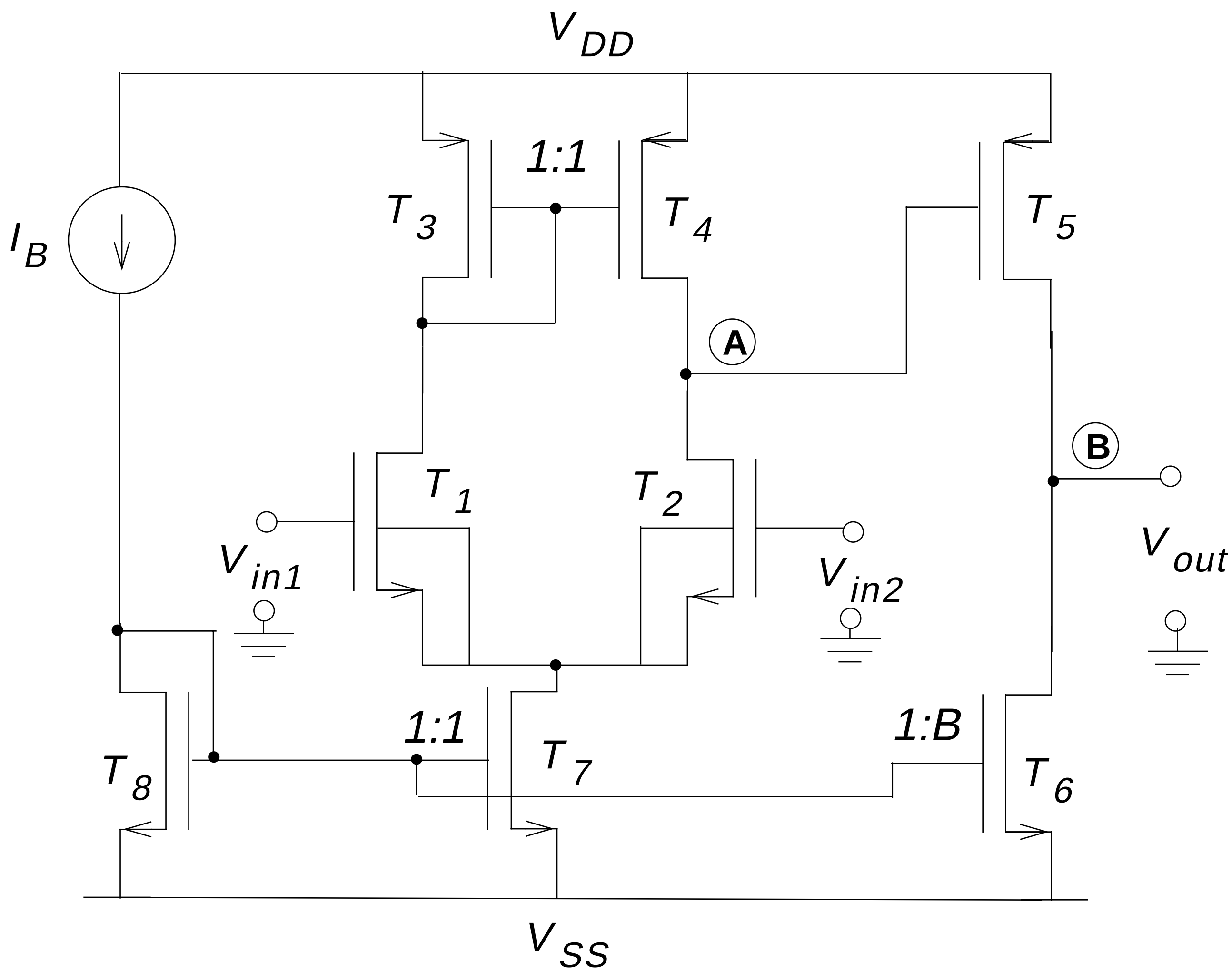
But maximum is rather flat.

A better choice in terms of area is:

$$\left(\frac{W}{L}\right)_l = 1 \Rightarrow \left(\frac{W}{L}\right)_i \approx 9.2$$

Finally, set I_B to max current that does not cause velocity saturation!

Two-stage amplifier

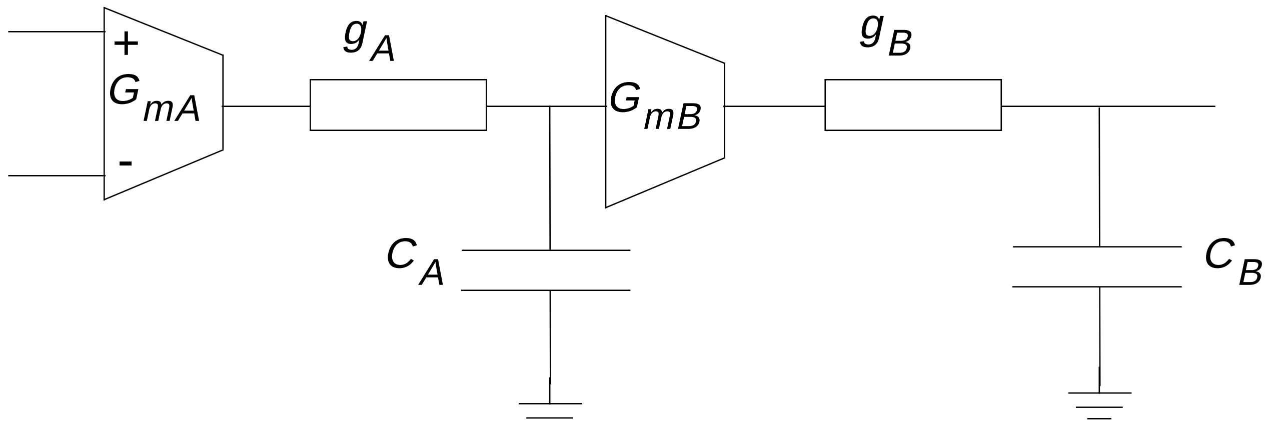


$g_{m1} = g_{m2} = g_{mi} \quad g_{m3} = g_{m4} = g_{ml}$

$g_{o1} = g_{o2} = g_{oi} \quad g_{o3} = g_{o4} = g_{ol}$

Two-stage amp block diagram

With two dominant poles:



First stage: $G_{mA} = g_{mi}$ $g_A = g_{oi} + g_{ol}$ $C_A = C_{D2} + C_{D4} + C_{parA}$

Second stage: $G_{mB} = g_{m5}$ $g_B = g_{o5} + g_{o6}$ $C_B = C_L + C_{D5} + C_{D6} + C_{parB}$

$$\frac{v_{out}}{v_{in}} = \frac{g_{mi}}{g_{oi} + g_{ol}} \frac{g_{m5}}{g_{o5} + g_{o6}} \frac{1}{\left(1 + \frac{sC_A}{g_{oi} + g_{ol}}\right)\left(1 + \frac{sC_B}{g_{o5} + g_{o6}}\right)}$$

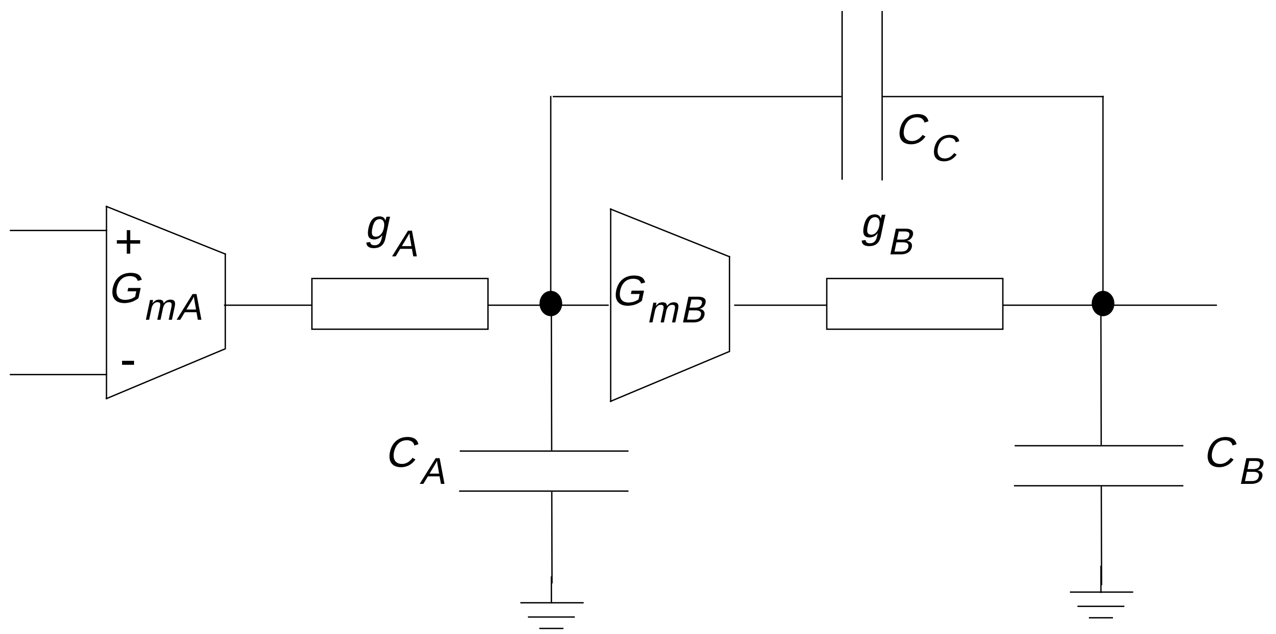
Note that there is really a third node/pole which could have some influence!

Compensation

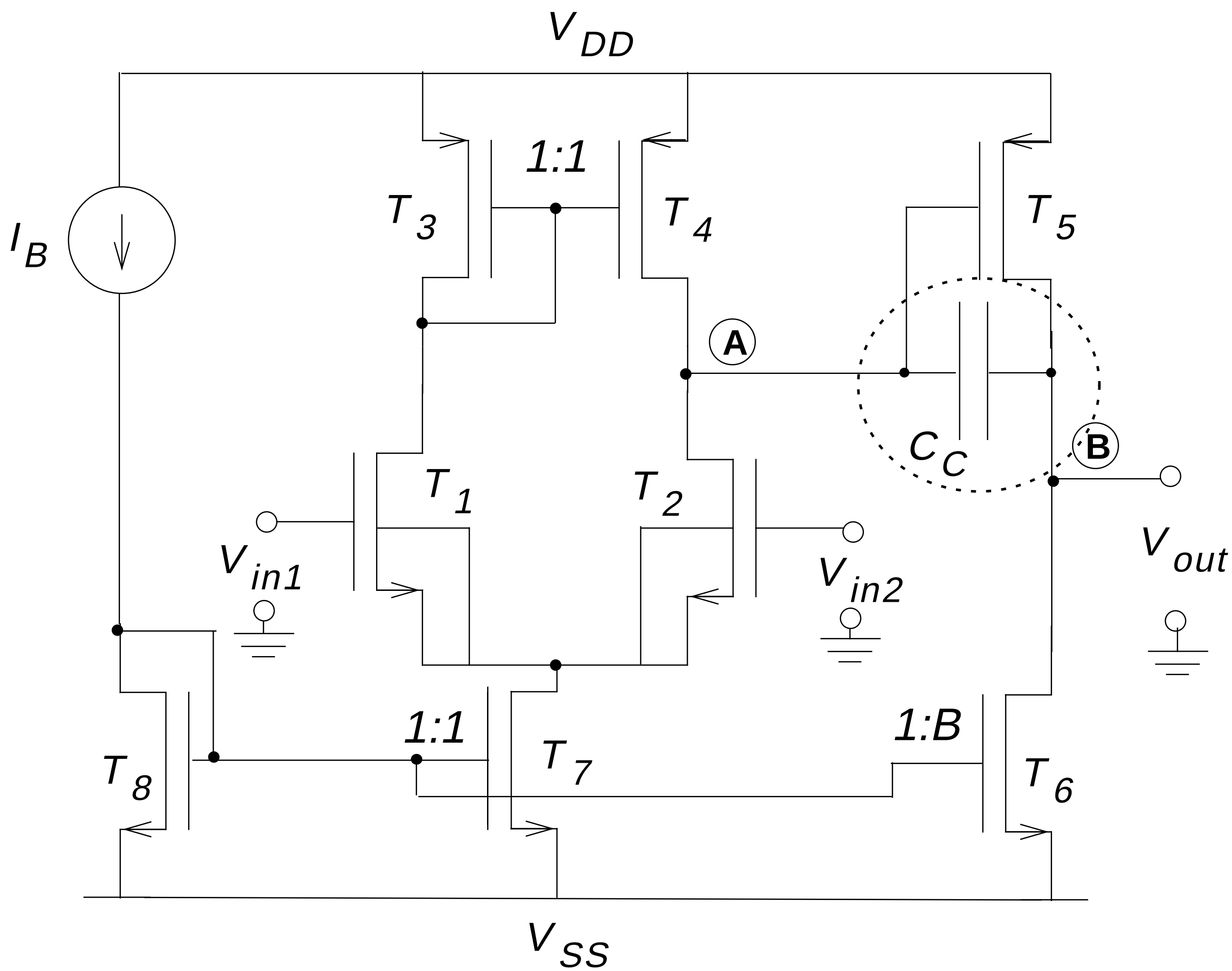
Can become unstable!

Move poles apart = compensate with polesplitting!

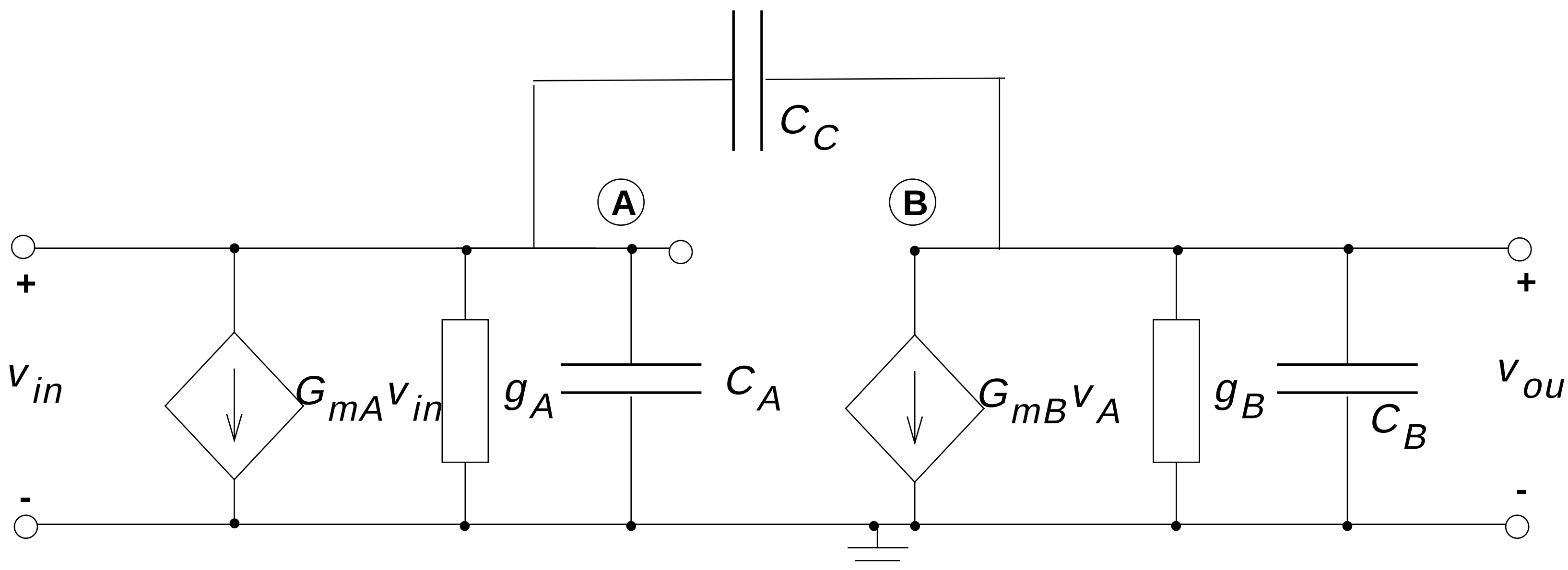
Usually g_m in stage 2 is already as high as possible - add compensation capacitor!



Schematic with compensation



Small-signal model



Looks very much like the common-source stage from last week!

Approximate poles:

Dominant pole at B:

$$f_d \approx \frac{1}{2\pi}\frac{g_A g_B}{G_{mB}C_c} = \frac{1}{2\pi}\frac{g_A}{A_{v0B}C_c}$$

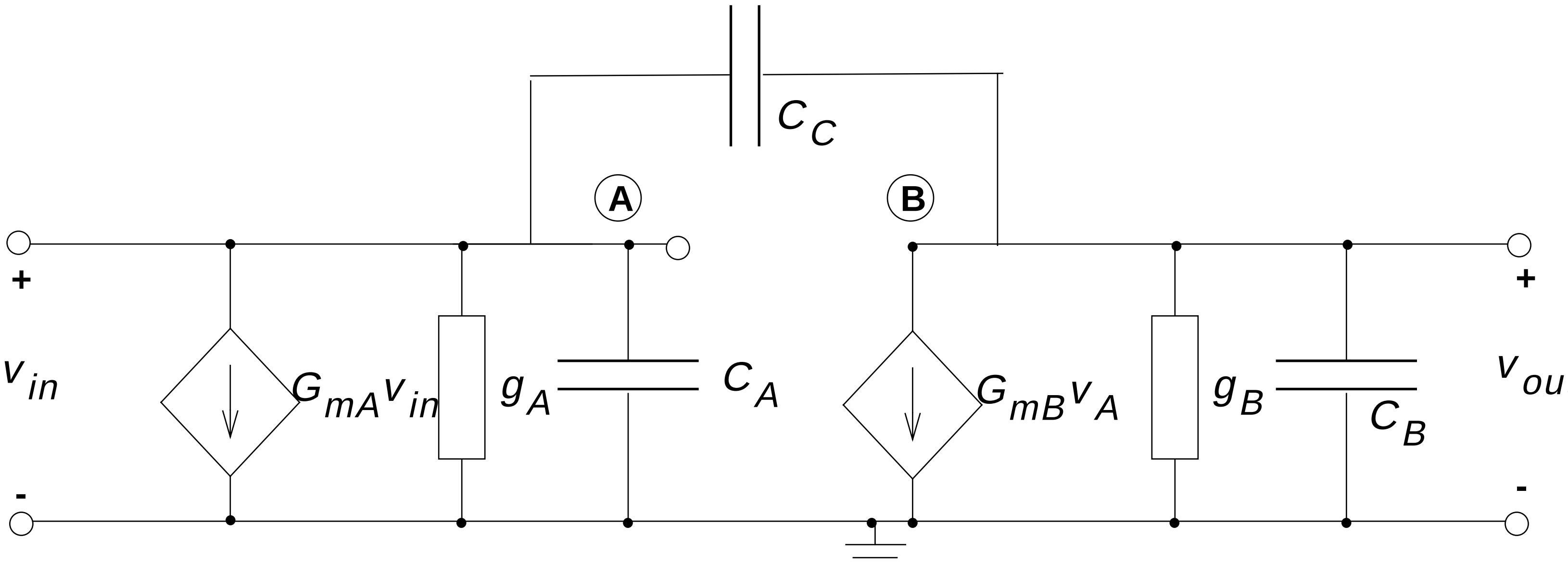
Miller cap!

Nondominant pole at A:

$$f_{nd} \approx \frac{1}{2\pi}\frac{G_{mB}C_C}{C_A C_B + C_C C_A + C_C C_B} \approx \frac{1}{2\pi}\frac{G_{mB}}{C_B}$$

If we assume: $C_A \ll C_B, C_C$

Example from textbook



First stage: $G_{mA} = 7.5\mu s$ $g_A = 0.03\mu s$ $C_A = 0.37pF$ $C_C = 1pF$

Second stage: $G_{mB} = 246\mu s$ $g_B = 11.8\mu s$ $C_B = 10.2pF$

No compensation: $f_{pA} = 13kHz$ $f_{pB} = 184kHz$

Compensation: $f_{pA} = 3.8MHz$ $f_{pB} = 229Hz$

Example Pole-zero & Bode diagrams

Positive zero

Total transfer function has this form:

$$A_v = A_{v0}\frac{1 - s\dfrac{C_c}{g_{mB}}}{1 + as + bs^2}$$

Zero in right half-plane gives negative phase addition:

Compensation of zero

If f_z is too close to f_{nd} the zero has to be moved further away

Add resistor R_z in series with compensation capacitor:

$$A_v = A_{v0} \frac{1 - sC_c\left(\frac{1}{g_{mB}} - R_z\right)}{1 + as + bs^2 + cs^3}$$

Move zero to infinity by setting R_z to $1/g_{mB}$

Resistor can be implemented by MOS transistor(s).

There are other schemes too outlined in textbook.

Design plan

- *Design specification:*
  - *gain-bandwidth*
  - *phase margin*
  - *something else*
  - *monitor other characteristics*
- *In Laker & Sansen: third spec is minimum area*
- *In lab: third spec is slew rate*

Design equations

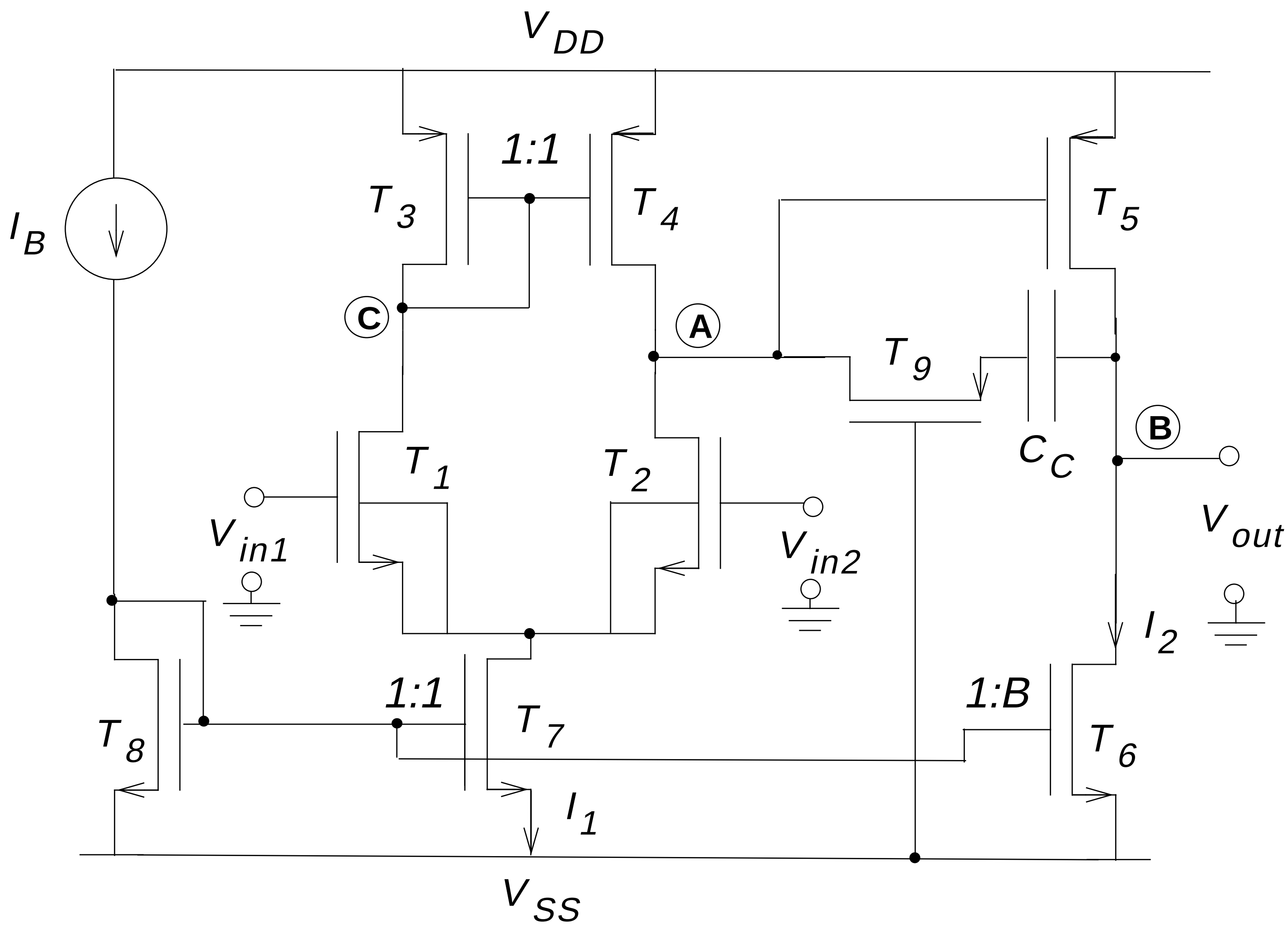
$$A_{v0} \approx \frac{G_{mA}G_{mB}}{g_A g_B} = A_{v0A}A_{v0B}$$

$$f_d \approx \frac{1}{2\pi}\frac{g_A g_B}{G_{mB}C_c} = \frac{1}{2\pi}\frac{g_A}{A_{v0B}C_c}$$

$$GBW \approx \frac{1}{2\pi}\frac{G_{mA}}{C_c}$$ *GBWeq.*

$$f_{nd} \approx \frac{1}{2\pi}\frac{G_{mB}C_C}{C_AC_B + C_CC_A + C_CC_B}$$ *ndeq.*

Schematic



V_{DD}
I_B
T_3
1:1
T_4
T_5
C
A
T_9
B
C_C
T_1
T_2
V_{in1}
V_{in2}
V_{out}
I_2
1:1
1:B
T_8
T_7
T_6
I_1
V_{SS}

Design plan with area as third spec

1. *Select a value for I_2 (free variable)*

2. *For T_6:*
   - *Choose V_{gs}-V_T = 0.2 V (for high gain)*
   - *Calculate g_{m6} and W/L_6*
   - *Choose minimum length for L_6*
   - *Calculate W_6*
   - *Calculate area for T_6*

3. *Repeat step 2 for T_5 with V_{gs}-V_T = 0.5 V or so*

4. *Calculate C_A from sizes of T6 and T5*

5. *Calculate C_C from ndeq (note: if selected I_2 is too small C_C becomes negative!)*

6. *Calculate area for C_C*

7. *Total area $A_T = A_5 + A_6 + A_C$*

Design plan cont.

Continue with input stage:

1. *GBWeq gives W/L_1 (= W/L_2). Large area is good here to minimize 1/f noise.*

2. *T_1 & T2: Select V_{GS}-V_T = 0.2 V since these transistors provide gain.*

3. *T_1 & T2: Now we can calculate current through T_1 (and T_2) and thus I_1*

4. *T_3 & T_4: For symmetry make sure both sides of diff pair has same DC voltage: V_C=V_A,V_C=V_{GS4}=V_{GS3}, and V_A=V_{GS6}=0.2 V + V_T determines sizes of T_3 and T_4.*

5. T_7: I_1 and $V_{GS7} = V_{GS5}$ determines size. Use same length as for T_5 for correct current scaling.

6. T_8: Same W and L as T_7 for matching.

7. T_9 (if necessary, check f_z relative f_{nd}):

$$R_z = \frac{1}{g_{o9}} = \frac{1}{g_{m5}}$$

T9 is in linear range because V_{DS9} is small while V_{GS9}-V_T is large.

$$V_{G9} = V_{SS}$$

$$V_{S9} = V_{DD} - V_{DS4} = V_{DD} - V_{GS4} = V_{DD} - 0.2V$$

$$\left(\frac{W}{L}\right)_8 = \frac{g_{m5}}{K_p'\left|V_{GS8} - V_{SS} - V_{Tp} - \gamma_p\left(\sqrt{\Phi_{bp} - V_{SB8}} - \sqrt{\Phi_{bp}}\right)\right|}$$

Slew rate

SR gives minimum bias current in both second and first stage:

Node A, T_2 discharging C_C:

$$SR_{int} = \frac{I_1}{C_C}$$

Node B, T_6 charging C_L and C_C

$$SR_{ext} = \frac{I_2}{C_L + C_C}$$

Example of SR dependence on C_L

Design plan with SR spec.

Choice of I_2 differs:

Generally $C_C <= C_L => SR^* C_L < I_2 < 2\ SR * C_L$

Make similar diagram as before (In your lab design currents smaller than around $1.4^*SR^*C_L$ will give negative values for C_C)

Then design plan is as before except that I_1 is defined by SR => V_{GS}-V_T for input transistors is not a design choice!

This is the only case when one does not want max g_m

Caveat

The design equation for f_{nd} is sensitive to actual cap values and they are not really known at start of design work

Therefore (and to account for parasitics etc.) one often chooses C_C from a rule of thumb to be on the safe size

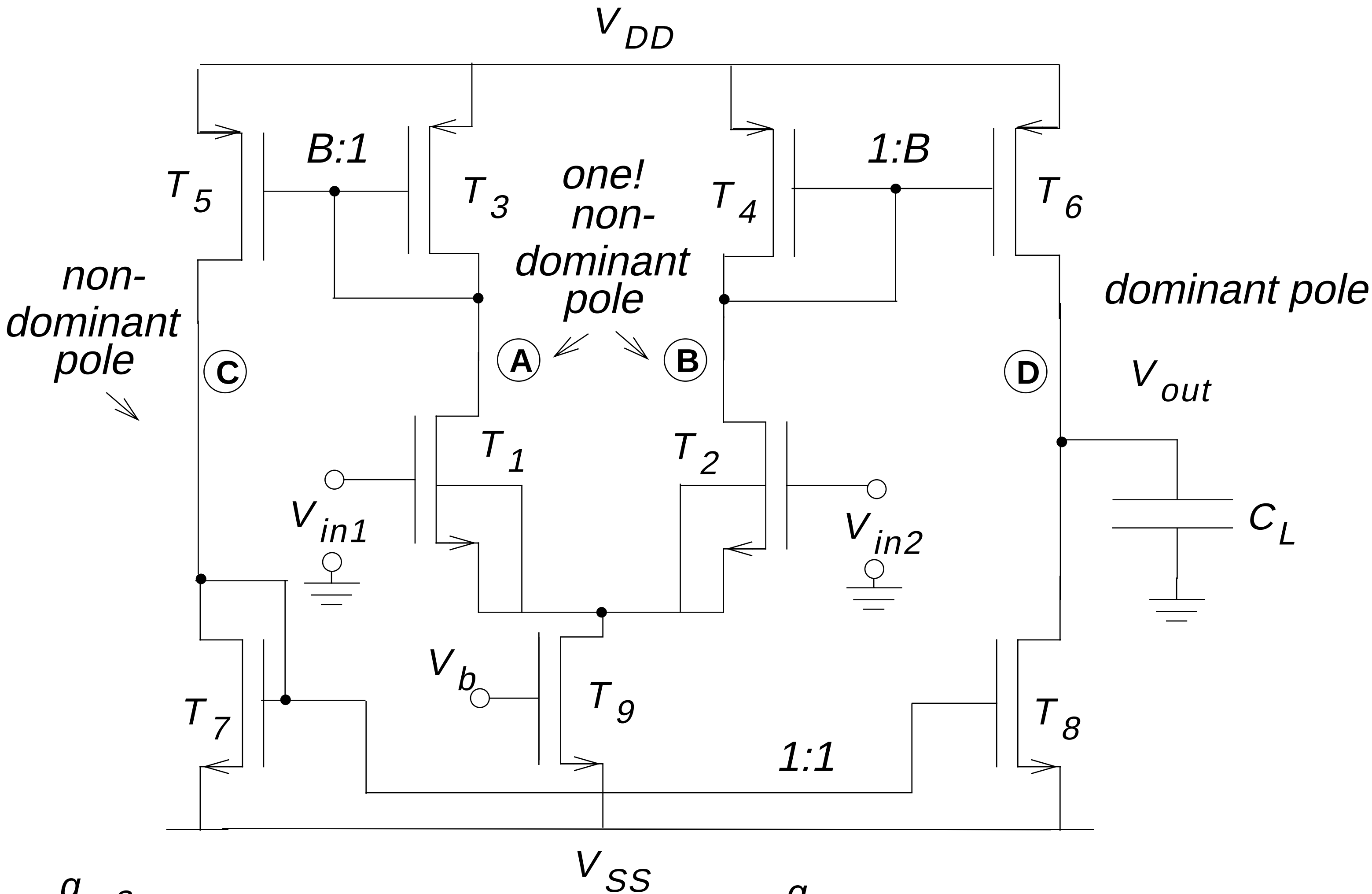
A general rule is to choose $0.5C_L <= C_C <= C_L$

If desired & possible C_C may be lowered later during design optimization

Symmetrical CMOS OTA

- *Mirrored version of simple OTA*
- *One dominant pole from the start*
  - *Load capacitance determines dominant pole*
  - *No compensation needed*
- *Open-loop gain much lower than for two-stage OTA*
- *Somewhat higher gain than for simple OTA*
  - *Better dynamic range!*

Symmetrical CMOS OTA schematic



$B = \frac{g_{m3}}{g_{m5}}$ improves slew rate $\quad A_{v1} = \frac{g_{m1}}{g_{m3}}$ improves noise perf.

GBW

$$A_{v0} = B\frac{g_{m1}}{g_D} = B\frac{g_{m1}}{2g_{o6}}$$

$$g_{m1} = \sqrt{2K_n'\left(\frac{W}{L}\right)_1 I_B} \qquad 2g_{o6} = \frac{BI_B}{V_{Ep}L_6} = \frac{BI_B}{V_{En}L_8}$$

$$A_{v0} = V_{Ep}L_6\sqrt{\frac{2K_n'}{I_B}\left(\frac{W}{L}\right)_1}$$

$$f_d = \frac{1}{2\pi 2g_{o6}(C_D + C_L)} = \frac{1}{2\pi 2g_{o6}C_L'}$$

$$GBW = \frac{Bg_{m1}}{2\pi C_L'}$$

Nondominant poles

*Nodes A and B cause **one** pole because of symmetry:*

$$f_{ndA} \approx \frac{g_{m3}}{2\pi C_A} = \frac{\sqrt{2K_p'\left(\frac{W}{L}\right)_3 I_B}}{2\pi C_A}$$

Node C causes a pole-zero doublet because node acts on only half the signal (see L&S appendix 6-1):

$$f_{ndC} \approx \frac{g_{m7}}{2\pi C_C} = \frac{\sqrt{2K_n'\left(\frac{W}{L}\right)_7 B I_B}}{2\pi C_C}$$

$$f_{zC} = 2 \cdot f_{ndC}$$

Note that the zero is negative -> positive phase addition

Pole-zero doublet illustration

Phase margin

$$f_{ndA} = M_A \cdot GBW \qquad f_{ndC} = M_C \cdot GBW$$

$$PM = 90° - \operatorname{atan}\frac{1}{M_A} - \operatorname{atan}\frac{1}{M_C} + \operatorname{atan}\frac{1}{2M_c}$$

$$M_A = \frac{f_{ndA}}{GBW} = \frac{1}{B}\frac{g_{m3}}{g_{m1}}\frac{C_L'}{C_A} = \frac{1}{BA_{v1}}\frac{C_L'}{C_A}$$

$$M_C = \frac{f_{ndC}}{GBW} = \frac{1}{B}\frac{g_{m7}}{g_{m1}}\frac{C_L'}{C_C}$$

How to increase PM:

Decrease B
Decrease C_C and C_A
Increase gm_7 (that is W/L_7)

(assuming C_L and A_{v1} fixed)

In general: Low B and A_{v1} is good for stability!

Design plan with SR and A_{V0} spec.

1. *Choose B and A_{v1} to reasonable values. Compromise between stability, noise performance and slew rate. Laker & Sansen says B=1-3 and A_{v1}=3-5. Max B is good for slew rate.*

2. *From SR calculate I_B:$SR=BI_B/C_L$ (neglect C_D)*

3. *T_1 & T_2: GBW gives g_{m1} (neglect C_D)*

4. *T_1 & T_2: I_B and g_{m1} gives W/L_1*

5. *T_3 & T_4: A_{v1} and g_{m1} gives g_{m3}*

6. *T_3 & T_4: I_B and g_{m3} gives W/L_3*

7. *T_5 & T_6: B and g_{m3} gives gm_5*

8. T_5 & T_6: BI_B and g_{m5} gives W/L_5.

9. T_5 & T_6: L_6 is given by A_{v0} equation.

10. T_8 & T_7: For balance at output node must have $V_{DS6} = V_{DS8}$. This gives W/L_8

11. T_8: & T_7: $L_8 = (V_{en}/V_{ep})L_6$ to match output conductances.

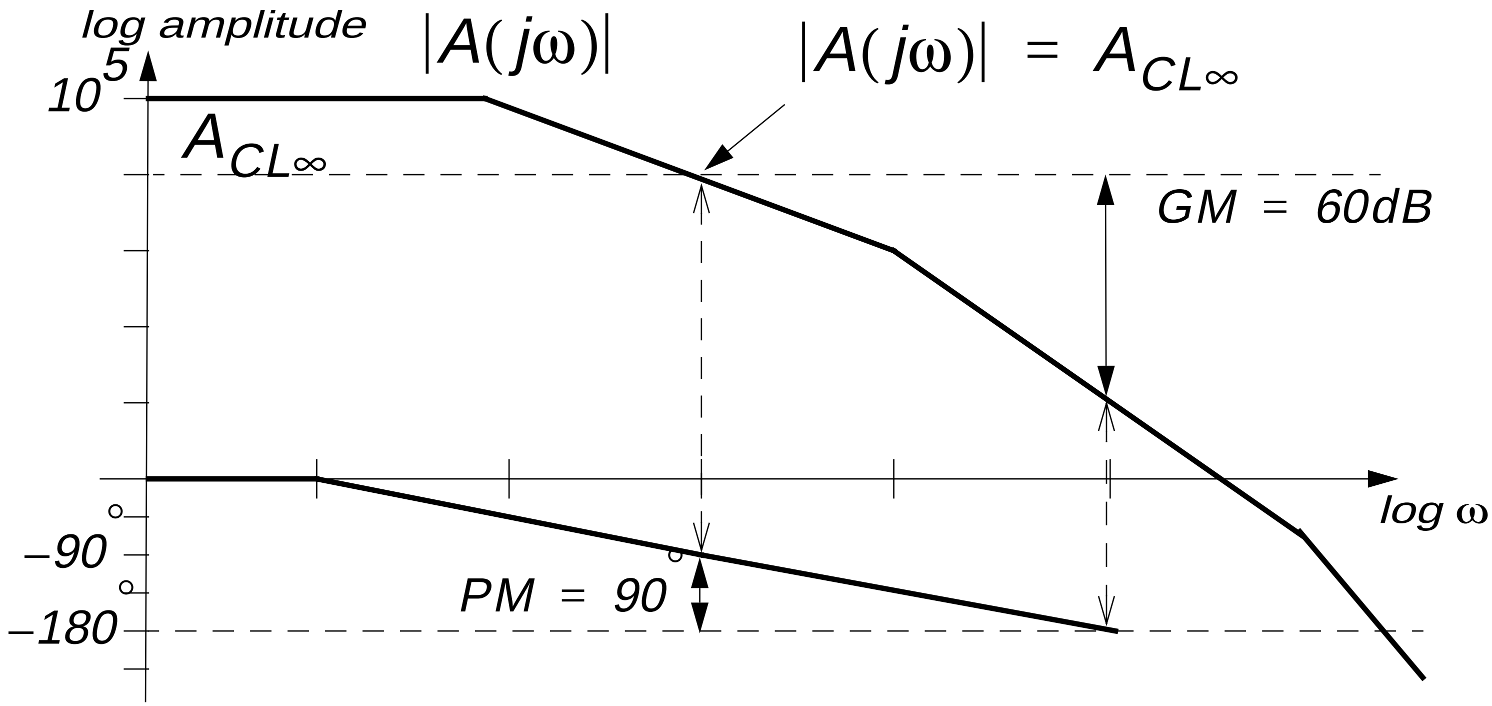
12. All that remains is the current source.

13. If T_8 and T_6 become to large then I_B must be increased instead to increase gain. A problem with making the output transistors long is that capacitance at nondominant poles increases -> stability deteriorates.

14. If necessary iterate until all design criteria are fulfilled!

A comment about GBW design spec.

GBW is "the" design criterion because follower configuration (closed-loop gain=1) is the worst case feed-back case:



Note: Some high-performance OPamps are designed to be stable only for closed-loop gains > 10 or so.